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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,380	11/12/2003	Cliff Hou	TS01-1674	6372

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,380	HOU ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Sano et al (USP 6651224)

(Claims 1, 5, 9, 13, 17, 21)

Allocating at least one delaying circuit within each of functional circuits (fig 1-2, 12, 15-35, 52, 62);

Fabricating an intra-functional clock distribution network within each of the functional circuits (fig 1-2, 12, 15-35, 52, 62);

Fabricating an inter-functional clock distribution network (fig 12, 21, 23, 24, 49-52, 62) between each of the functional circuits;

Determining a clock skew for the inter-functional clock distribution network (technical field, background, disclosure, fig 1, 4, 7, 10-35, 36, 41-42, 49-52, 62); and

Compensating for the clock (skew) of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-functional clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network (fig 1-2, 12, 15-35, 52, 62).

(*For "synthesizing a clock distribution circuit" in claim 17, technical field, background, fig 1, 3, 21, 49-50, best mode for carrying invention (col 17)*)

(Claims 2, 6, 10, 14, 18, 22) determining a clock skew factor for one selected functional circuit connected to one selected terminal of inter-functional clock distribution network (technical field, background, disclosure, fig 1, 4, 7, 10-35, 36, 41-42, 49-52, 62); and adjusting the delaying circuit within

said one selected functional circuit to cancel out said clock skew factor (technical field, background, disclosure, fig 1, 4, 7, 10-35, 36, 41-42, 49-52, 62).

(Claims 3, 7, 11, 15, 19, 23) wherein said delaying circuit includes a plurality of delaying buffer circuits, each delaying buffer circuit having a first increment of delay (fig 1-2, 15-22)

A plurality of interconnect wiring segments placed between each of the plurality of delaying buffer circuits, said interconnecting wiring segments having a second increment of delay (fig 4, 7, 10-14, 21, 25, 36, 41, 49-52)

(Claims 4, 8, 12, 16, 20, 24) wherein adjusting said delaying circuit comprising the step of Connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnect wiring segments such that a sum of the first increment of delay of said first quantity of the delaying buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor (fig 1-2, 4, 7, 10-36, 41, 49-52, 62)

2. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Teng et al (USP 6751786)

(Claims 1, 5, 9, 13, 17, 21)

Allocating at least one delaying circuit (delaying circuit = buffer/driver in subtrees T1-T4 of fig 9-10) within each of functional circuits (P1-P4);

Fabricating an intra-functional clock distribution network (T1-T4) within each of the functional circuits;

Fabricating an inter-functional clock distribution network (top level clock tree 18 in fig 9) between each of the functional circuits;

Determining a clock skew for the inter-functional clock distribution network (fig 8-10, col 6-8); and

Compensating for the clock (skew) of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-functional clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network (fig 8-10, col 6-8).

(*For "synthesizing a clock distribution circuit" in claim 17, see fig 7-8*)

(Claims 2, 6, 10, 14, 18, 22) determining a clock skew factor for one selected functional circuit

connected to one selected terminal of inter-functional clock distribution network (fig 8-10, col 6-8); and adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor (fig 8-10, col 6-8).

(Claims 3, 7, 11, 15, 19, 23) wherein said delaying circuit includes a plurality of delaying buffer circuits (fig 9-10), each delaying buffer circuit having an first increment of delay ("larger size/number of buffer" col 3, "increase/adjust the size and/or number of buffers" (col 7); and

A plurality of interconnect wiring segments placed between each of the plurality of delaying buffer circuits (fig 9-10), said interconnecting wiring segments having a second increment of delay (by increasing/adjusting paths/interconnects/segments/length/width/thickness (fig 8-10, col 6-8))

(Claims 4, 8, 12, 16, 20, 24) wherein adjusting said delaying circuit comprising the step of Connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnect wiring segments such that a sum of the first increment of delay of said first quantity of the delaying buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor (fig 8-10, col 6-8 teach this limitation, i.e., by increasing/adjusting buffer size and/or number and paths/interconnects/segments/length/width/thickness to match/balance/adjust/cancel clock delay/skew)

3. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Yonemori (USP 6609241)

(Claims 1, 5, 9, 13, 17, 21)

Allocating at least one delaying circuit within each of functional circuits (see arrange/add/insert buffer in macros in fig 2-5, 7);

Fabricating an intra-functional clock distribution network within each of the functional circuits (fig 2-5, 7, clock buffers in macros);

Fabricating an inter-functional clock distribution network (top level clock tree synthesis (CTS), top level clock wiring/paths/buffer in fig 2-3, buffer 5 in fig 7) between each of the functional circuits;

Determining a clock skew for the inter-functional clock distribution network (abstract, background, summary, fig 2-3, 5, 7); and

Compensating for the clock (skew) of said inter-functional clock distribution network by inserting said delaying circuit at a terminal of said inter-functional clock distribution network where each of said functional circuits is connected to said inter-functional clock distribution network (fig 2-3, 5, 7).

(*For "synthesizing a clock distribution circuit" in claim 17, see fig 2-3, 5*)

(Claims 2, 6, 10, 14, 18, 22) determining a clock skew factor for one selected functional circuit connected to one selected terminal of inter-functional clock distribution network (abstract, background, summary, fig 2-3, 5, 7); and adjusting the delaying circuit within said one selected functional circuit to cancel out said clock skew factor (abstract, background, summary, fig 2-3, 5, 7).

(Claims 3, 7, 11, 15, 19, 23) wherein said delaying circuit includes a plurality of delaying buffer circuits (fig 2-3, 5, 7), each delaying buffer circuit having a first increment of delay (fig 2-3, 5, 7, by increase/adjust the size/number/fanout load of buffer)

A plurality of interconnect wiring segments placed between each of the plurality of delaying buffer circuits (fig 2-8), said interconnecting wiring segments having a second increment of delay (by determining increasing/adjusting paths/interconnects/segments/length/width/thickness at top level (fig 2-8))

(Claims 4, 8, 12, 16, 20, 24) wherein adjusting said delaying circuit comprising the step of Connecting a first quantity of said delaying buffer circuits with a second quantity of said plurality of interconnect wiring segments such that a sum of the first increment of delay of said first quantity of the delaying buffer circuits and the second quantity of delay of said interconnecting wiring segments is equal to the clock skew factor (fig 2-8 teach this limitation, i.e., by arranging increasing/adjusting buffer size/number/load fanout/location and paths/interconnects/segments/length/width/thickness to match/balance/adjust/cancel clock delay/skew)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner